Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A method of forming a damascene interconnect barrier layer, the method comprising:

forming a trench in a dielectric layer;

implanting Ca ions into the sidewalls of the trench;

forming a seed layer over implanted sidewalls in the trench; and

forming an inlaid metal conductor on the seed layer in the trench.

Claim 2 (original): The method as recited in claim 1 wherein the Ca ion implantation is conducted using a series of tilted implants.

Claim 3 (original): The method as recited in claim 2 wherein the series of tilted calcium ion implantations is conducted at a wafer tilt angle ranging from about 0 to 30° and twist angle increments of 90° per rotation.

Claim 4 (original): The method as recited in claim 1 wherein the calcium ion implantation generates a calcium concentration profile extending from the surface of the trench sidewall to a depth up to 500 Angstroms.

Claim 5 (original): The method as recited in claim 1 wherein the calcium ion implantation generates a peak calcium concentration to a depth in the range from about 50 to 500 Angstroms from the surface of the trench sidewall.

Claim 6 (previously presented): The method as recited in claim 2 wherein the series of tilted calcium ion implants is conducted such that about 25% of calcium is implanted in said trench sidewalls for a given twist angle.

Claim 7 (previously presented): The method as recited in claim 2 wherein the series of tilted calcium ion implantation steps are conducted at about a 90° angle to the surface of the substrate.

Claim 8 (original): The method as recited in claim 1 further comprising implanting a concentration of calcium ions into the bottom of the channel using a straight implant.

Claim 9 (original): The method as recited in claim 1 further comprising forming a second calcium ion implanted layer above the top surface of the inlaid metal conductor wherein said second calcium ion implantation is conducted with Ca ions using 10 to 80keV energy.

Claim 10 (original): The method as recited in claim 9 wherein said second calcium ion implantation is conducted with Ca ions using from 10 to 20keV of the ion energy (or acceleration energy) and a 0 to 30° tilt.

Claim 11 (original): The method as recited in claim 9 wherein said second calcium ion implantation is conducted with a $1x\ 10^{14}cm^{-2}$ to $1x\ 10^{16}cm^{-2}$ of ion dose.

Claim 12 (original): The method as recited in claim 9 wherein said second calcium ion implantation is formed in a low-k layer disposed directly on the top surface of the inlaid conductor.

Claim 13 (original): The method as recited in claim 12 wherein the low-k layer has a thickness in the range from about 10 to 500 Angstroms.

Claim 14 (original): The method as recited in claim 9 wherein the inlaid conductor is copper and said second calcium ion implantation is formed directly on the top surface of the inlaid conductor.

Claim 15 (original): The method as recited in claim 1 wherein the trench is formed in a single damascene process.

Claim 16 (original): The method as recited in claim 1 wherein the trench is formed in a dual damascene process.

Claims 17 & 18 (cancelled).

Claim 19 (currently amended): ~~The integrated circuit as recited in claim 18 further comprising~~ **A semiconductor integrated circuit comprising:**

a dielectric layer having a channel formed therein;

a seed layer formed in the channel;

an inlaid copper conductor formed on the seed layer in the channel of the dielectric layer;

a first calcium implant region comprising a concentration of Ca atoms incorporated into the sidewalls of the channel under the seed layer using ion implantation; and

a second calcium ion implanted region formed in a low-k layer disposed directly on the top surface of the inlaid conductor.

Claim 20 (cancelled).